Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.011”**

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**.011”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .003” x .003” min.**

**Backside Potential: COLLECTOR**

**Mask Ref: CP392V**

**APPROVED BY: DK DIE SIZE .011” X .011” DATE: 6/2/22**

**MFG: CENTRAL SEMI THICKNESS .008” P/N: 2N3904**

**DG 10.1.2**

#### Rev B, 7/19/02